**Clock Module Description Document**

1. **Introduction**

The Clock of the AP80 series chips has three sources: RC48M, LP32K, and OSC32K/xMHz. Among them, RC48M and LP32K are both inside the chip, while OSC32K/xMHz are sourced from the outside.

The reason for the existence of RC48M is that to achieve rapid power-on, the external crystal oscillator at 32KHz takes 2 seconds to start oscillating, which is unacceptable. The stabilization time of RC48MHz is only 10 microseconds. So within the two seconds required for the OSC to vibrate, the chip needs to rely on the RC48MHz clock to do a lot of work.

The LP32K is provided to the LP(low power) module during the time when the osc32K is not powered on. When the software controls the switch to the OSC32K, it will be automatically turned off.

OSC32K/xMHz, as the primary Clock source for the AP80 chip, needs to select its frequency based on the external crystal oscillator's frequency under RC48M. It can accept external input frequencies ranging from 32.768KHz to 1MHz. After the selection is completed, the software needs to switch from RC48MHz to DPLL.

**2.RC48M Description**

Modules that can operate normally under RC48M include:

Watchdog，PWM，CTS，IR，rst\_ctrl(por)，Wakeup，FSHC，PHUB，dlut，DMA，LCD，SD，SPIM，SPIS，drmc，Cache，GPIO。

Points to note：

1.The Decoder module cannot decode normally after its frequency is halved.

2. mclk\_12m becomes 2 MHZ under RC48M.

3. The accuracy of RC48M may not meet the requirements of Uart (2% to 3%), so compensation needs to be calculated using the internal OSC/RC48MHz.

4.Clock may be lost when switching clocks, which could affect the PWM waveform.

5. The clock of the Watchdog is only provided by RC48M.

6.Timer0/1 needs to be adjusted before it can work properly

**3.DPLL Description**

OSC32K/xMHz is doubled to 480M by DPLL and then downclocked to generate five clocks: 48M, 60M, 80M, 96M and 12.288M.

1.The 60M clock is only provided for the USB and FSHC modules.

2. The FSHC module can operate with four types of clocks: 48M, 60M, 80M, and 96M respectively.

3. The clock of the Uart module has two sources: one is 96M generated by DPLL, and the other is RC48M. Not affected by frequency division.

4. MCLK has three sources. One is 12.28M generated by DPLL, and depending on different sampling rates, it can also generate 11.2896M. The other one can be injected from the outside. Another one is the 12M of 96M generated by DPLL after 1/8 division, or the 2M of RC48M after 1/3 division and 1/8 division

5. At the beginning of power-on, the LP module is provided with the Clock by RC32K. Once the Clock is switched by software control, it is directly provided by OSC32K, and RC32K is automatically turned off.

6. The clocks directly provided by OSC32K include scan\_clk and LP modules.

7. Clock usage of the remaining modules not affected by system frequency division:

* The PWM and CTS modules are independent 12M and are not affected by frequency division.
* The IR and rst\_ctrl(por) modules are independent 50K and are not affected by frequency division.
* wakeup is an independent 500Hz frequency and is not affected by frequency division.

8.Clock usage of the remaining modules affected by system frequency division:

* The three modules of PHUB, SPIS and Decode operate on a 12M clock.
* Seven modules, namely Dlut, DMA, LCD, drmc, Cache, Timer0 and Timer1, operate on a 96M clock.
* The two modules, SD and SPIM, operate on a 48M clock.
* All register configurations are 12M clocks

1. **Clock Module Functions**

1. Supports independent enable and disable of clock for each module, or full enable/disable. When certain modules are not in use, their clocks can be disabled to reduce power consumption.

2. Supports independent control of dynamic clockgating for each module, or full enable/disable.

3.Supports selection of different generation modes for mclk.

4. Supports selection of different mclk according to different sampling rates.

5. Supports generating 12M or 16M clock for external use.

6. Supports switching the clock from DPLL to RC48M during operation, and also supports switching from RC48M to DPLL during operation.

7. Supports system clock frequency division.

8. Supports the system to obtain the current system operating frequency at any time after DPLL stabilization.

9. Supports crystal oscillator capacitor-free function.